

**ANSALDO****Ansaldo Trasporti s.p.a.**  
**Unita' Semiconduttori**Via N. Lorenzi 8 - I 16152 GENOVA - ITALY  
Tel. int. +39/(0)10 6556549 - (0)10 6556488  
Fax Int. +39/(0)10 6442510  
Tx 270318 ANSUSE I -**PHASE CONTROL THYRISTOR****AT681**

Repetitive voltage up to	<b>6000 V</b>
Mean on-state current	<b>840 A</b>
Surge current	<b>10 kA</b>

**FINAL SPECIFICATION**

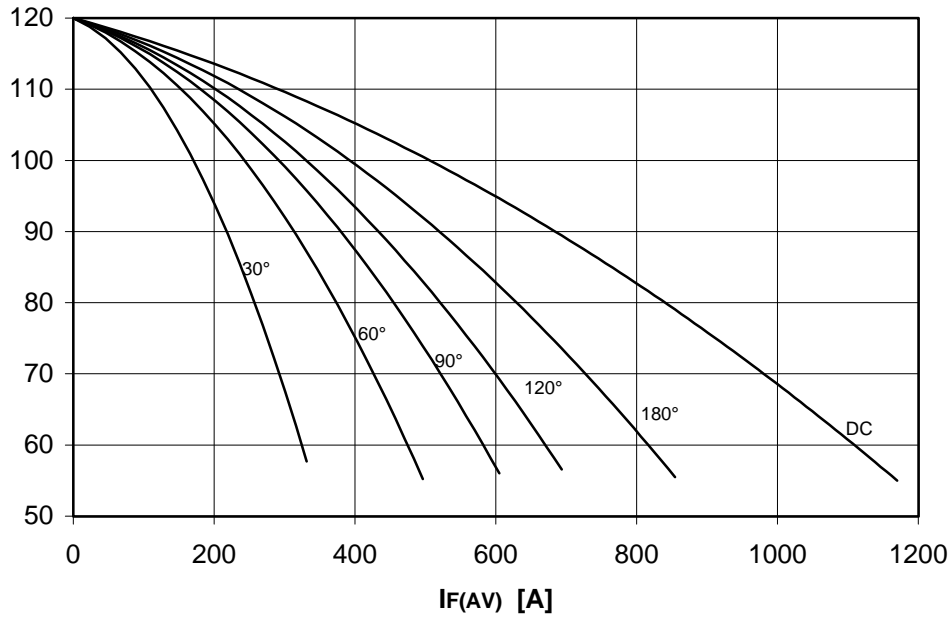
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Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub>	Repetitive peak reverse voltage		120	6000	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		120	6100	V
V <sub>DRM</sub>	Repetitive peak off-state voltage		120	6000	V
I <sub>RRM</sub>	Repetitive peak reverse current	V=V <sub>RRM</sub>	120	150	mA
I <sub>DRM</sub>	Repetitive peak off-state current	V=V <sub>DRM</sub>	120	150	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		840	A
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		705	A
I <sub>TSM</sub>	Surge on-state current	sine wave, 10 ms	120	10	kA
I <sup>2</sup> t	I <sup>2</sup> t	without reverse voltage		500 x1E3	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 1570 A	25	2.4	V
V <sub>T(TO)</sub>	Threshold voltage		120	1.3	V
r <sub>T</sub>	On-state slope resistance		120	1.150	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current	From 75% V <sub>DRM</sub> up to 1200 A	120	100	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 75% of V <sub>DRM</sub>	120	500	V/μs
t <sub>d</sub>	Gate controlled delay time, typical	V <sub>D</sub> =200V, gate source 20V, 10 ohm	25	5	μs
t <sub>q</sub>	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 80% V <sub>DRM</sub>		650	μs
Q <sub>rr</sub>	Reverse recovery charge	di/dt=-60 A/μs, I <sub>s</sub> = 1000 A	120		μC
I <sub>rr</sub>	Peak reverse recovery current	VR= 50 V			A
I <sub>H</sub>	Holding current, typical		25	300	mA
I <sub>L</sub>	Latching current, typical		25	700	mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage		25	3.5	V
I <sub>GT</sub>	Gate trigger current	V <sub>D</sub> =5V	25	400	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	0.5 V <sub>DRM</sub>	120	0.5	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			5	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			2	W
<b>MOUNTING</b>					
R <sub>th(j-h)</sub>	Thermal impedance, DC	Junction to heatsink, double side cooled		21	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, double side cooled		6	°C/kW
T <sub>j</sub>	Operating junction temperature			120	°C
F	Mounting force			22.0 / 24.5	kN
	Mass			520	g
<b>ORDERING INFORMATION : AT681 S 60</b>					
standard specification <input type="checkbox"/> VDRM&VRRM/100 <input type="checkbox"/>					

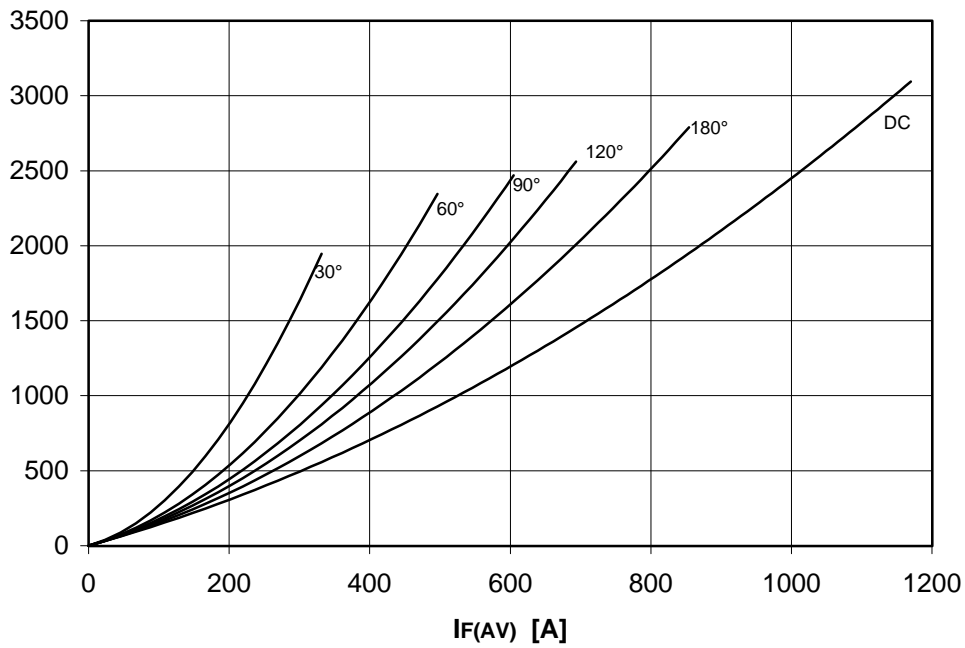
DISSIPATION CHARACTERISTICS

SQUARE WAVE

Th [°C]



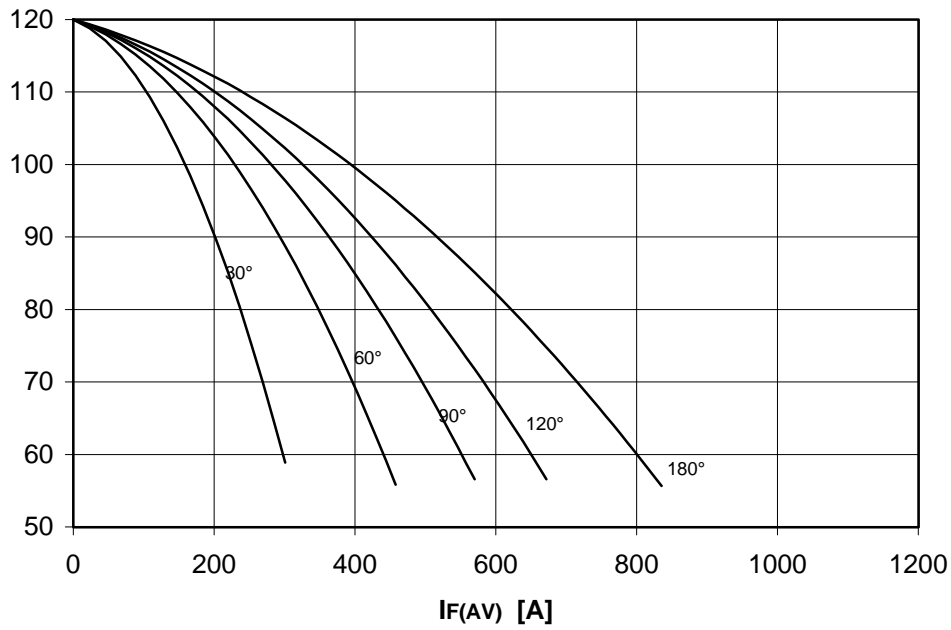
PF(AV) [W]



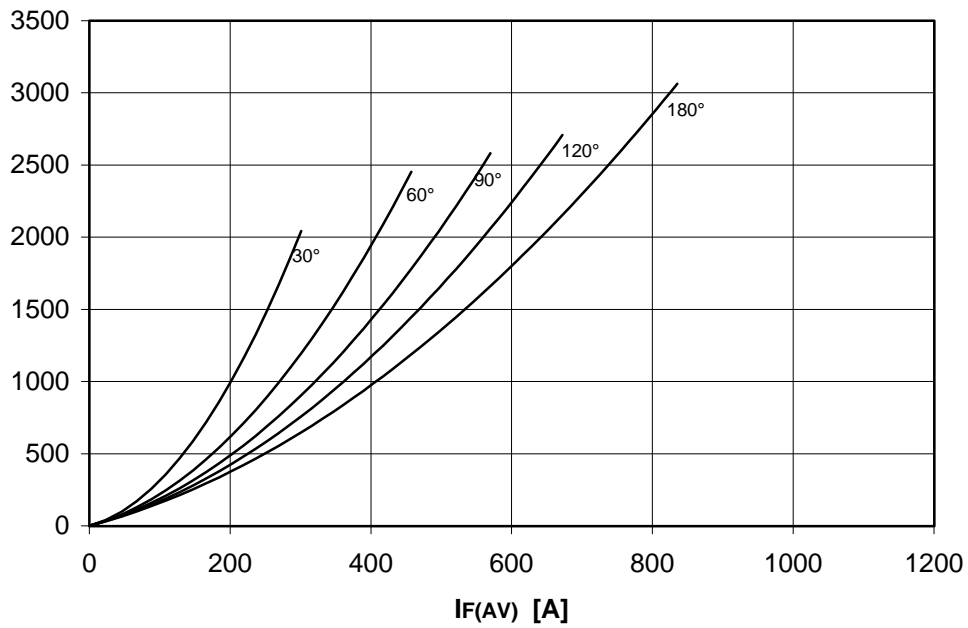
**DISSIPATION CHARACTERISTICS**

SINE WAVE

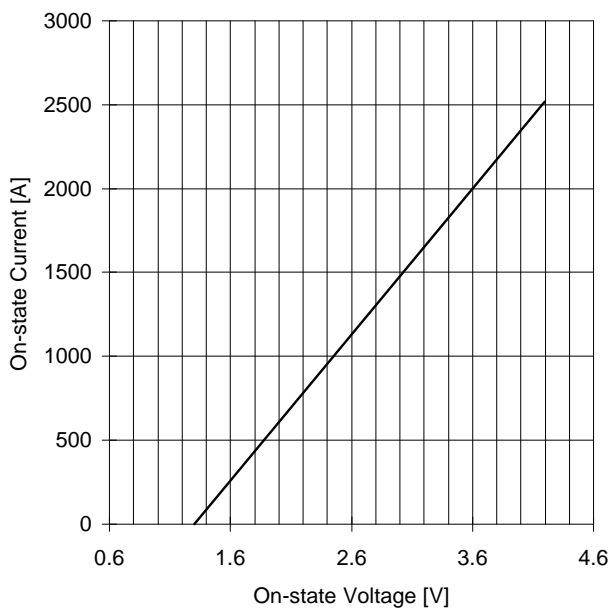
**Th [°C]**



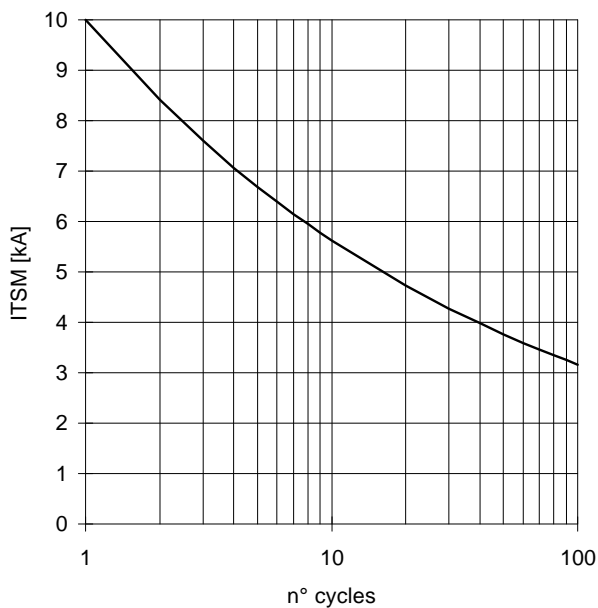
**PF(AV) [W]**



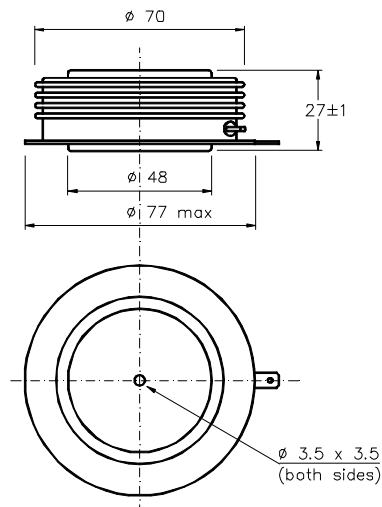
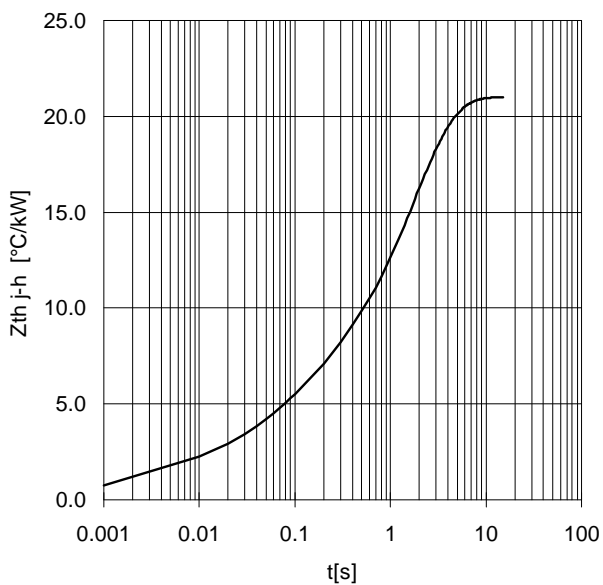
ON-STATE CHARACTERISTIC  
T<sub>j</sub> = 120 °C



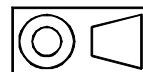
SURGE CHARACTERISTIC  
T<sub>j</sub> = 120 °C



TRANSIENT THERMAL IMPEDANCE  
DOUBLE SIDE COOLED



Dimensions  
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2  $\mu\text{m}$ .

In the interest of product improvement ANSALDO reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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